

# Investigation of Millisecond-Long Analog Single-Event Transients in the LM6144 Op Amp

Y. Boulghassoul, *Student Member, IEEE*, S. Buchner, *Member, IEEE*, Dale McMorrow, V. Pouget, L. W. Massengill, *Senior Member, IEEE*, P. Fouillat, W. T. Holman, *Member, IEEE*, C. Poivey, *Member, IEEE*, J. W. Howard, *Senior Member, IEEE*, M. Savage, *Member, IEEE*, and M. C. Maher, *Senior Member, IEEE*

**Abstract**—A new category of analog single-event transients (SETs) with millisecond-long durations have been experimentally observed in the LM6144 operational amplifier. It is the first time that events with such extreme widths are under investigation in a linear integrated circuit. Relying on heavy-ion broadbeam tests, picosecond pulsed lasers diagnostics, and computer-assisted circuit modeling, we uncover the mechanisms and causes of these anomalous voltage transients. The identification of the problematic area of the IC reveals that the bias/startup circuitry is sensitive to energetic ionizing particles and can be responsible for corrupted circuit operations when subjected to a heavy-ion strike. A circuit hardening solution with minimal impact on the layout and the electrical performances of the op amp are proposed to mitigate this effect.

**Index Terms**—Analog single-event transients, heavy-ion broadbeam, LM6144 operational amplifier, millisecond pulse width, multistable circuit, picosecond pulsed laser, radiation hardening by design.

## I. INTRODUCTION

THE PROCESS of radiation qualification of commercial off-the-shelf (COTS) parts for spacecraft on-board integration benefits greatly from the variety of investigative tools presently available. The traditional heavy-ion broadbeam testing for single-event transients (SETs) has been supplemented with the picosecond pulsed laser for single-photon

absorption [1], the ion microbeam [2], the femtoseconds laser for two-photon absorption (TPA) [3], and computer simulation [4]. By combining results and observations from various sources, experimental tests can provide valuable insights into the SET phenomenon and its effects on the response of integrated circuits under ionizing particle irradiation.

It is in this framework that we are investigating a new and potentially critical category of analog SETs: voltage transients with pulse widths exceeding the millisecond range, that is, pulse durations several orders of magnitude longer than anything previously reported in the literature. The unexpected occurrences of such long-duration pulses (LDPs) were first recorded during a heavy-ion broadbeam campaign on the LM6144 operational amplifier, and later on, confirmed through extensive picosecond pulsed laser investigations on the IC.

ASETs with such extreme characteristics can have catastrophic effects in space systems. From the time domain perspective, because of their width, they are more likely to corrupt the signal for a considerable number of clock cycles and disrupt any functions requiring synchronized operations. In the frequency domain, their predominant low-frequency spectra make them much harder to filter than their high-frequency counterparts, allowing them to propagate to any subsequent circuitry without effective attenuation.

In this paper, we present the experimental effort that was conducted to quantify this anomalous ASET response of the LM6144. The heavy-ion broadbeam data, postprocessed into full width at half maximum (FWHM) plots, singled-out the ASET subset of concern and underlined its unique characteristics. Also, picosecond pulsed lasers were effectively employed for ASET investigations, as they succeeded in 1) localizing the sensitive part of the IC responsible for the LDP generation and 2) decoupling several triggering conditions that modulated the ASET pulse width duration.

Then, we combine computer simulations with the experimental observations to explain the correlation between heavy-ion strikes and losses of functionality experienced by the LM6144. ASET circuit simulations on the transistor-level model of the IC are used to expose the primary failure mechanism responsible for LDP origination and help analyze the secondary processes behind the nuances in the experimental results. This allowed us to present a simple design option for improving the radiation hardness of the sensitive circuit. With minimal impact on the chip area and

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Y. Boulghassoul, L. W. Massengill, and W. T. Holman are with Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, TN 37235 USA.

S. Buchner is with the National Aeronautics and Space Administration (NASA)/Goddard Space Flight Center (GSFC) and QSS, Seabrook, MD 20706 USA.

D. McMorrow is with Naval Research Laboratory, Washington, DC 20375 USA.

V. Pouget and P. Fouillat are with IXL Microelectronics Laboratory, Université Bordeaux 1, 33405 Talence Cedex, France.

C. Poivey is with National Aeronautics and Space Administration (NASA)/Goddard Space Flight Center (GSFC) and SGT, Greenbelt, MD 20771 USA.

J. W. Howard is with National Aeronautics and Space Administration (NASA)/Goddard Space Flight Center (GSFC) and Jackson & Tull, Greenbelt, MD 20771 USA.

M. Savage is with NAVSEA, Crane, IN 47522 USA.

M. C. Maher is with National Semiconductor Corporation, South Portland, ME 04106 USA.

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on the electrical performances of the IC, this solution can have potential applications to circuit topologies presenting multistable radiation-sensitive operations, as it was determined to be the case for the LM6144 op amp.

## II. HEAVY-ION EXPERIMENTS

The device under test was the LM6144 analog operational amplifier from National Semiconductor Corporation [5]. It has been designed for use in applications requiring low voltage supplies with strict power consumption restrictions like battery operated systems and wireless communications. Therefore, the LM6144 has been considered as a potential candidate for space deployment and it was during a broadbeam ion test campaign that it exhibited an ASET response with pulse widths as long as 1.5 ms. This duration is up to three orders of magnitude longer than previous pulse durations observed in analog ICs.

### A. Experimental Details and Broadbeam Results

In previous heavy-ion broadbeam tests, analog ICs commonly exhibited ASET pulse widths ranging from hundreds of nanoseconds for comparators to tens of microseconds for operational amplifiers [6], [7], and hardness assurance methodologies were developed accordingly [8]. So, the recording of ASETs with pulse width exceeding the millisecond range, during tests conducted at the Texas A&M cyclotron facility, came as a surprise and raised serious concerns. Fig. 1 shows a sample of the heavy-ion test results on the LM6144 where the IC response is exhibiting LDPs [7]. The device under test (DUT) was exposed to the heavy-ion beam delidded and the circuit configuration used was an inverting configuration with a closed loop gain of 10 V/V, an input voltage of 650 mV, and with power supplies set to  $V_{CC} = -V_{SS} = 10$  V.

In Fig. 1(a) are plotted four oscilloscope recordings presenting the evolution of LDPs at the output of the LM6144. We see that the transient perturbation of the output voltage is gradually increasing, followed by a fast saturation of the ASET amplitude, while the pulse width keeps extending past 50  $\mu$ s (initial capture limit of the oscilloscope) to reach the most extreme value of 1.5 ms. Fig. 1(b) shows all the ASETs recorded in the described circuit configuration, but this time plotted using the FWHM representation. The FWHM representation was adopted as a standard for plotting the ASET response of an IC: each dot has for coordinates the voltage amplitude of a recorded ASET and its pulse width at half of maximum amplitude. This representation outlines the very unique trend of long-duration ASETs (subset D), clearly distinguishable from the more classical ASET signatures: fast bipolar, fast positive, and fast negative pulses (subsets A, B, and C, respectively).

### B. Preliminary Analysis

Pertinent information on the LDPs can be obtained from the analysis of the heavy-ion broadbeam data:

- 1) The LDP subset (D) only appeared when the LM6144 was exposed to high-LET Xe and Au, with a bracket of LETs ranging from 49.99 to 93.27 MeV  $\text{cm}^2/\text{mg}$  [7]. This indicates that the generation of LDPs is tightly related to the proprieties of such heavy particles (i.e., amount of deposited charge, track structure, and range).

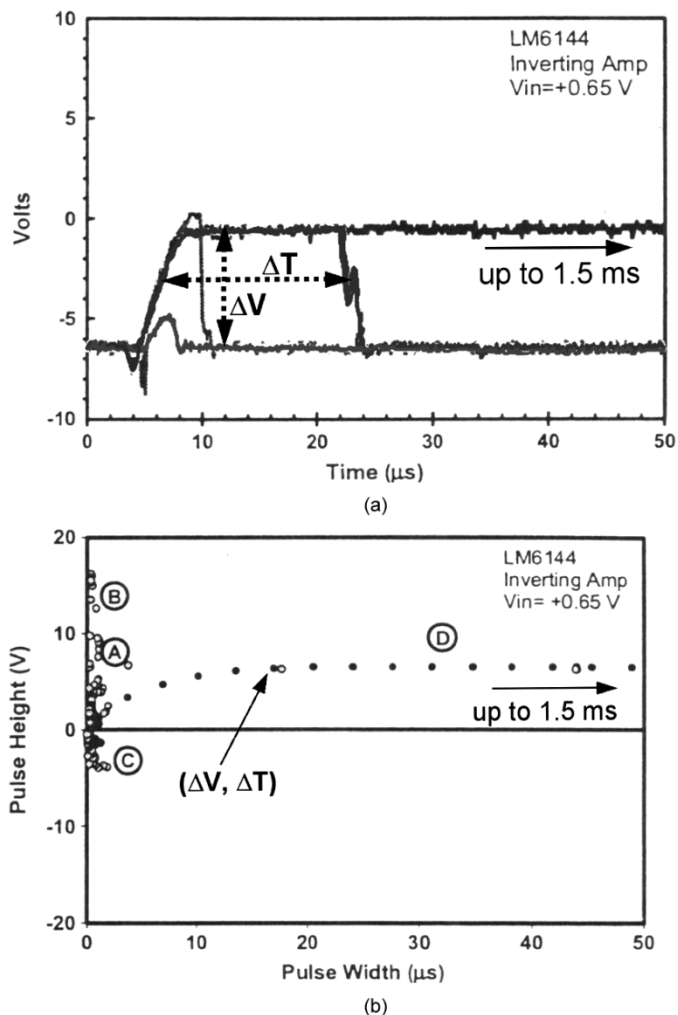


Fig. 1. Heavy-ion test results on the LM6144 op amp: (a) oscilloscope recording of the LDPs at the LM6144 output and (b) representation of the recorded ASETs using the FWHM format, showing the distinct characteristic of the LDPs (subset D).

- 2) In contrast with previously published ASET data where saturating transients had their amplitudes limited by the power supply rails (or at some diode voltage drops below), the LDPs seem to saturate at intermediate voltages bearing minimal correlation (if any) with the supply voltages as Fig. 1(a) shows. So LDPs are no regular ASETs, simply propagating as voltage/current glitches and resulting in a transient alteration of the conduction state of downstream active elements. We are facing a problem that originates at a higher circuit level.
- 3) We know from previous ASET work that the “branches” in the FWHM representation can be precisely mapped back to specific areas on the IC under tests. So what first looked like a random scattering of plots can be read as a dynamic evolution of the ASET sensitivity of individual transistors. From Fig. 1(b), we can see that the LDP subset is the only branch that exceeds the 4  $\mu$ s value of pulse widths. The absence of overlapping with other trends strongly hints that a very specific area of the chip may be responsible for these long transients.

At this stage of our analysis, we hit a roadblock inherent to heavy-ion broadbeam testing: the randomness of the ion strikes

provides only a global statistical observation of the ASETs at the output terminal of the DUT. To proceed further in our analysis of the LDP phenomenon, we will use the picosecond laser unique ability to add a spatial resolution to our investigation.

### III. LASER EXPERIMENTS

Following the observation of extreme LDP events during the heavy-ion tests, laser experiments were conjointly performed at the IXL laboratory and at the NRL pulsed laser SEE test facility to further investigate the phenomenon. The IXL picosecond pulsed laser is tunable from 750 nm to 1050 nm and was set to 800 nm and 900 nm during the tests. The NRL picosecond pulsed laser has a fixed wavelength of 590 nm. The IXL and NRL laser setups are described in [1] and [9]–[11], respectively.

#### A. Sensitive Area Identification and LDP Replication

The pulsed laser was scanned across the entire surface of the chip, with a relatively high pulse energy of 80 pJ, in an attempt to locate the areas responsible for the LDP generation. The longer wavelength (900 nm) was used first since it provides a more comfortable  $1/e$  penetration depth of 30  $\mu\text{m}$  for triggering deeply originated mechanisms. The laser illumination of only a very localized part of the IC (approximately  $3.10^{-4} \text{ cm}^2$ ) induced long output transients comparable to those obtained during the heavy-ion tests: two NPN transistors in the bias/startup circuitry of the LM6144. If the laser struck any of these two transistors, the output voltage would enter the LDP latched-like state. Fig. 2 shows the location of the sensitive area on the chip from which it was possible to identify the transistors responsible for the anomalous ASETs.

In Fig. 3, we present a typical circuit response of the LM6144 after a laser strike on the sensitive transistors. The external circuit conditions were as follow: inverting configuration, closed loop gain of 10 V/V (10 k $\Omega$  for the feedback resistor), input voltage of  $-60 \text{ mV}$ , and  $V_{cc} = -V_{ss} = 10 \text{ V}$ . We can see that the output voltage of the LM6144 abruptly drops by 0.6 V as soon as the laser strikes occurs (the temporal resolution of the laser is monitored through the signal of a photodiode). The output voltage needs more than 25 ms to recover its initial steady state value. Also, it was noticed that the recovery time exhibited a dependence on the supply voltage amplitude set during the irradiation: the smaller the power supplies, the longer the recovery time needed (25 ms, 45 ms, and 100 ms for  $V_{cc} = -V_{ss} = 10 \text{ V}$ , 7.5 V, and 5 V, respectively). So, in addition to the precise identification of the sensitive area on the surface of the IC, the laser was also successful in qualitatively replicating the LDP phenomenon. We must however note that the width of the laser-induced LDPs is significantly longer than the broad-beam-induced ones. We will address this discrepancy in our discussion.

#### B. Investigation of LDP's Triggering Conditions

With the sensitive area identified, several additional tests were performed with wavelengths of 800 nm and 590 nm, to understand the triggering conditions of the LDPs as well as the mechanisms modulating the output voltage recovery. We present here the highlights of these experiments.

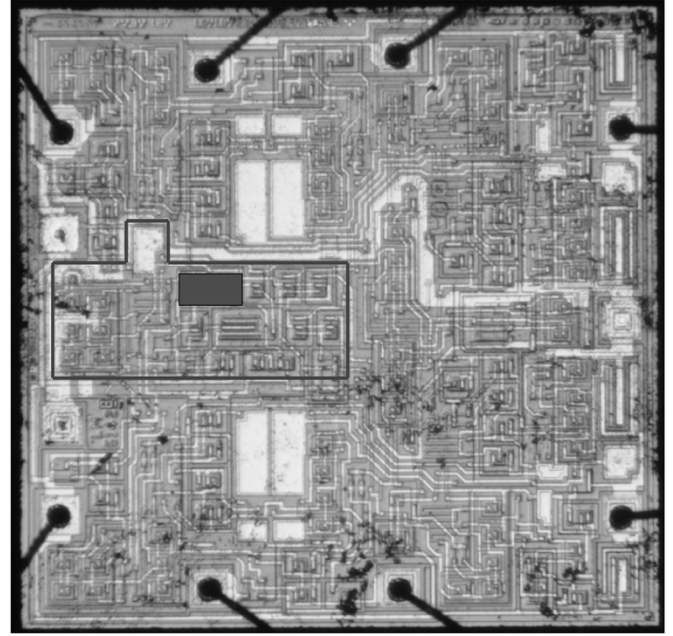


Fig. 2. Photomicrograph of one of the two LM6144 dies, containing two amplifiers each. The shaded area marks the region where LDPs were generated by laser strikes while the delimited portion of the layout constitutes the bias/startup circuitry of the IC.

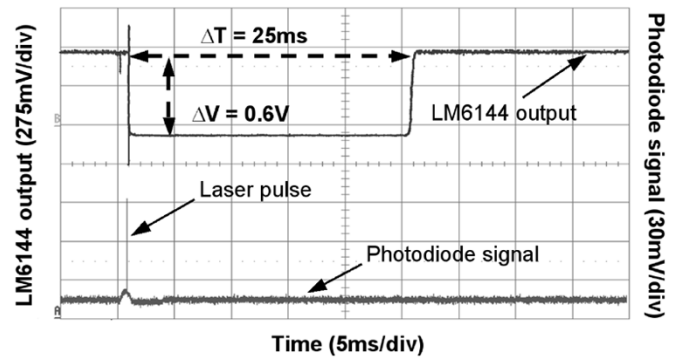


Fig. 3. Recording of a LDP at the output of the LM6144 following a laser strike on the sensitive area.

- 1) After focusing the laser beam on the sensitive area, the illuminator light used to view the chip on the monitor was turned off and the half-wave plate was rotated until the beam had a minimum intensity (note that no neutral density filters were used to reduce the intensity of the beam). Starting from this LDP-free condition, the intensity of the laser light was gradually increased by rotating the half-wave plate until LDPs were observed. Reducing the laser light intensity to its original minimum level by rotating back the half-wave plate did not remove the LDPs. The beam had to be completely blocked to have the output voltage recover.
- 2) Now, with the illuminator turned ON to its lowest setting and its light further attenuated (by inserting an opaque material) to such a degree that the features on the chip could barely be seen on the monitor, we gradually increased the

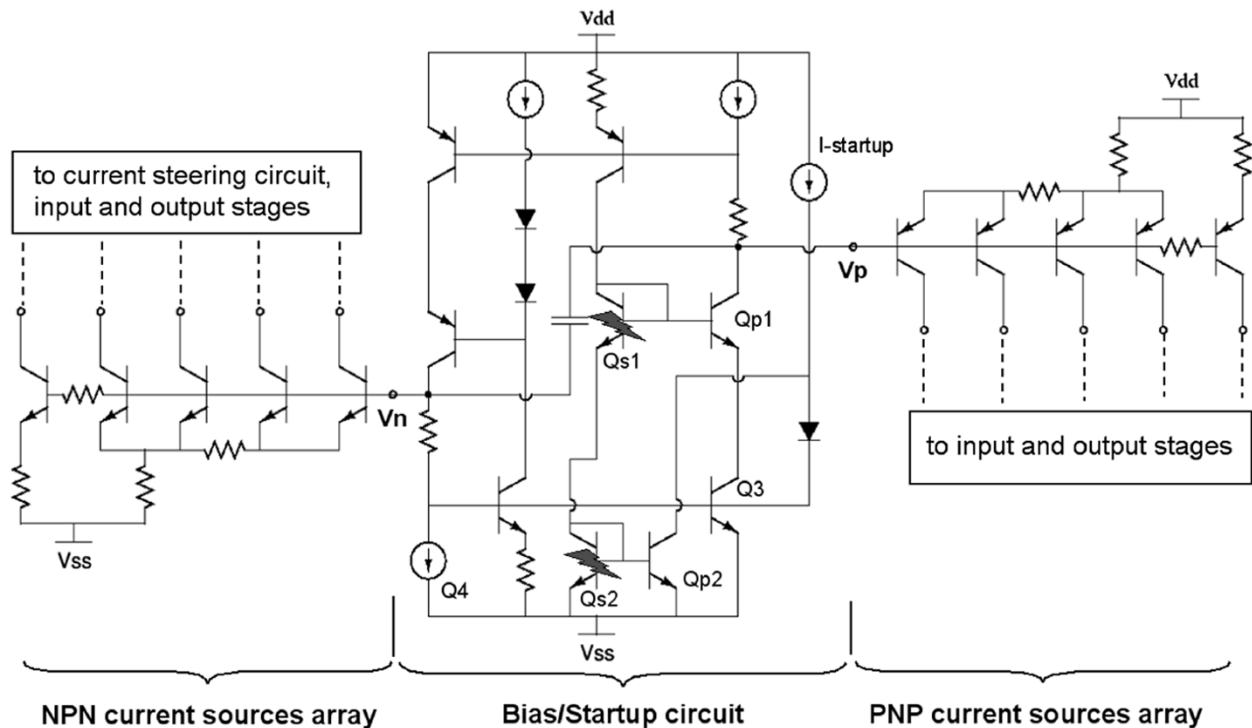


Fig. 4. Simplified schematic of the LM6144 bias/startup block. For circuit design proprietary reasons, several elements are replaced by their purpose-equivalent current sources. The two sensitive NPN transistors (Qs1 and Qs2) are also indicated.

laser light intensity until a LDP was produced. Reducing the laser intensity to its original minimal value, and even completely blocking the beam did not make the LDP disappear. This condition was only achieved when the illuminator light was also turned off.

- 3) This time, a lens with a longer working distance was used, exposing the sensitive part to more room light. After generating a LDP with the laser, we blocked both the laser beam and the light from the illuminator. To our surprise, the LDP did not disappear; it only did when the room lights were turned off.
- 4) Finally, after producing an LDP with the laser, we moved the beam and focused it outside—but in the vicinity—of the sensitive region. The LDP immediately disappeared, regardless of the surrounding lights that were still on.

### C. Complementary Analysis

The results of these investigations suggest that the LDPs have several properties.

- 1) A relatively high laser beam intensity is needed to produce the LDPs. This agrees with the broadbeam data where LDPs were only observed for the high-LET ions of Au and Xe.
- 2) No influence of the wavelength on the preceding properties was observed for the three wavelengths used in this work. It implies that the penetration depth of approximately  $1.5 \mu\text{m}$  corresponding to the shorter wavelength (590 nm) is sufficient for triggering an LDP.
- 3) Once an LDP is generated, a small amount of light can significantly delay the circuit recovery toward pre-irradiation biases. The parasitic light can be produced by the

illuminator light used to view the chip on the monitor, the scattered light in the laser beam and even the room light of the experimental facilities.

- 4) If the output of the LM6144 is experiencing an LDP, a laser strike on a transistor adjacent to the sensitive NPN transistors will induce a premature recovery, even when they are exposed to background light.

From the experimental results, a hypothesis linking the latch-like response exhibited by the LM6144 to a functional perturbation of the bias/startup block is starting to emerge. In the following part, we use circuit inspection and computer simulation to demonstrate that the LDPs are due to a parasitic radiation-induced bistable state, prompting the LM6144 into unreliable electrical operations.

## IV. LDPs CIRCUIT SIMULATIONS

To expose the radiation-induced mechanisms at play, the purpose of the bias/startup block must be first understood and its topology examined.

### A. Background and LDP Mechanism Hypothesis

A startup circuit is usually used for circuits that may present two or more stable operating states at power-on, that is, power can be switched ON but the transistors of the circuit can stay off or set themselves in an operating mode different from the one required by the designer. From our inspection of the LM6144 schematic (a simplified version is presented in Fig. 4), such a situation can happen to the biasing circuitry, where several key transistors stay in the OFF conduction state: Q3, Q4, Qp1, and consequently Qs1, Qs2, and Qp2. Therefore, the inclusion of a startup circuit—in this case a field-effect transistor acting as a

current source ( $I$ -startup), forcing the transistors to go into the proper operating mode as soon as the power is turned on. Here, a base current is forced into Q3 and Q4, turning both transistors slightly on. This allows the PNP transistors to start conducting, which in turn provides base current to Qs1, Qp1, Qs2, and Qp2. With increased collector current provided by Qp1, Q3 turns fully on and is soon followed by the other transistors, with the initial  $I$ -startup no longer actively participating to the biasing of the circuit and being now redirected to  $V_{ss}$  through Qp2.

Based on the numerous experimental observations, our hypothesis of the LDP mechanism is that the exposure to a high-energy laser beam (or very energetic ion) may act as a second startup current. In response to this parasitic photocurrent, the biasing circuitry enters an unintended stable biasing configuration, where its transistors are in the OFF conduction state, and where it can be maintained by a very small current (several feedback loops can be identified on the circuit schematic). Therefore, the circuit can remain latched until every photocurrent-generating source is turned off, allowing the photo-induced excess charges to leak out, the  $I$ -startup to reset the proper biasing, and the output voltage to recover.

### B. Simulation Diagnosis of Failure

Computer simulations have confirmed the hypothesis implicating the bias/startup circuitry as responsible for the LDP phenomenon. The simulation of heavy-ion strikes or laser illuminations at the sensitive locations forced the biasing circuitry into a parasitic state, where its transistors are experiencing a steady perturbation of biases. Such modifications are particularly noticeable at the two nodes acting as negative and positive outputs to the bias/startup block (refer to Fig. 4), and are of dire consequences to the proper electrical operation of the LM6144. The heavy-ion and laser-beam strikes were simulated by injecting transient photocurrents across desired transistor junctions, the integral profile of the current pulse providing an estimation of the total charge injected in the circuit. Since the response of the LM6144 showed little dependence on the current pulse profile, it can be modeled by a double exponential or a simple square wave pulse. We used the square wave option for ease of charge calculation.

From the circuit simulation results presented in Fig. 5(a) and (b), we can see that the immediate consequence of a strike on any of the two sensitive transistors is to induce an alteration of the voltages  $V_n$  and  $V_p$ :  $V_n$  changes from a pre-strike value of  $-9$  V to  $-9.25$  V while  $V_p$  increases from  $9.2$  V to  $9.8$  V (the injected current pulse had the following characteristics: collector-emitter strike,  $7$  mA  $\times$   $4.3$  ns =  $30$  pC). It is important to notice that these two nodal voltages have a direct control on the base-emitter voltages of NPN and PNP transistor arrays used as biasing current sources for the rest of the circuit. The change in the control voltages has a limited effect on the NPN array operation, but it is critical for the PNP array: the new SET-induced voltage is clearly insufficient to maintain the transistors in their pre-rad forward-active mode. Without the proper biasing currents provided by the PNP array, various circuit blocks of the IC lose their functionality, setting the output voltage to an erroneous value.

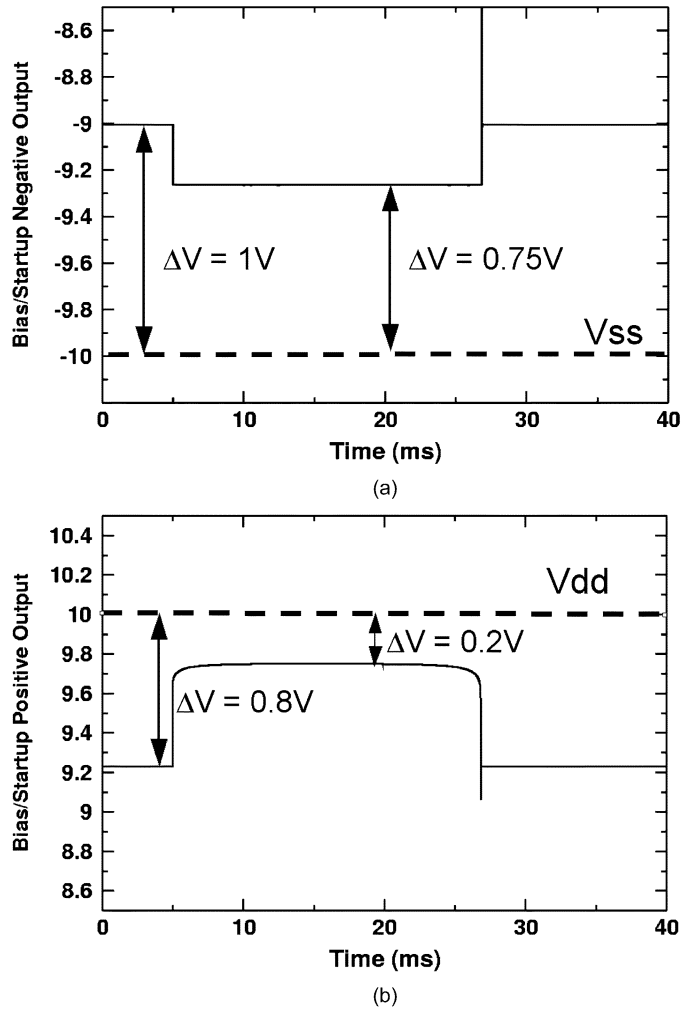


Fig. 5. Variations in the bias/startup output voltages  $V_n$  and  $V_p$  following a simulated laser strike. (a) The voltage available to the NPN's array is still sufficient to maintain proper BE junction biasing. (b) The voltage available to the PNP array drops below the minimum  $V_{be}$  required to keep the transistors on.

We can track the sequence of events behind the control voltages variations if we focus on the first few microseconds following the simulated laser strike and monitor the currents of the transistors Qs1 and Qp1 (Fig. 6): a hit on the sensitive transistor Qs1 depletes the paired transistor Qp1 from a portion of its base current  $I_{b\_Qp1}$  (due to the low impedance path created), in turn inducing a decrease in the collector current  $I_{c\_Qp1}$ . But, since the collector node is also coupled to a capacitor plate, we start to see some recovery in the current as the capacitor compensates for the sudden loss of charge.

However, a competing phenomenon is also taking place. The circuit is designed such that  $I_{c\_Qs1}$  is proportional to  $I_{c\_Qp1}$  (low-current biasing design configuration). When  $I_{c\_Qp1}$  first start decreasing,  $I_{c\_Qs1}$  also decreases. Doing so, it deprives even more the struck transistor from its proper biasing currents. A feedback action is then setting in, where even less base current is provided to the paired transistor, ultimately turning it off and having  $I_{c\_Qp1}$  go to zero. With no voltage drop across the resistor tied to the positive output node, the control voltage  $V_p$  drifts toward the power rail  $V_{dd}$  (the negative output voltage  $V_n$  drifts similarly toward  $V_{ss}$ ).

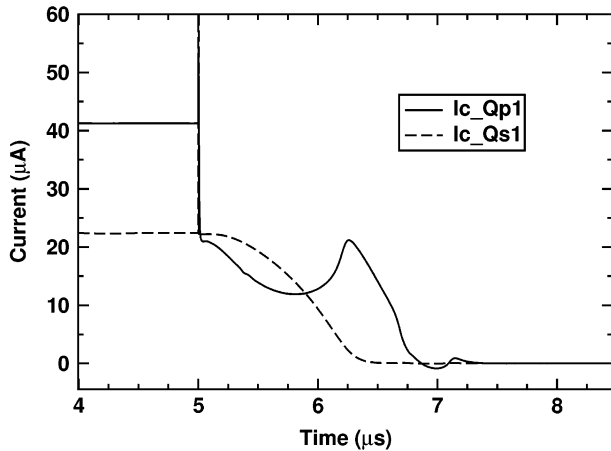


Fig. 6. Fluctuation of Qs1 and Qp1 collector currents after a simulated strike. Both currents ultimately settle to 0 A, which indicates that the transistors have turned off.

## V. DISCUSSION

With the identification of the main failure mechanism causing LDP generation, we are in a position to explain the details of the various experimental observations.

### A. High-LET-Induced Phenomenon

Both heavy-ion and laser experiments agreed that a high amount of charges needs to be generated in the sensitive region of the DUT for an LDP to appear. This is confirmed by SPICE circuit simulations, which required the integrated profile of the injected current pulse to be at least 20.5 pC so that an ASET with LPD characteristics is produced. Also, the simulated pulse had to be injected as a collector-emitter strike, modeling a shunt in the sensitive NPN transistor. This is consistent with the type of photocollection that we might expect from a high-LET ion or a high intensity laser beam, where the plasma of free carriers is dense and deep enough to shunt the narrow base region of vertical NPNs.

From the currents perspective, the monitoring of internal nodes showed that a perturbation of at least 45% of Qp1 quiescent base current was required to set the outputs of the bias/startup block into a corrupted state. Smaller perturbations result in Ic\_Qp1 recovery as opposed to the case in Fig. 6 where Qp1 ultimately turns off. However, the minimum current perturbation required decreases with smaller supply voltages, which is consistent with the fact that the circuit is operating at smaller quiescent currents. So we expect an increase in the IC cross-section with decreasing power supplies.

### B. Interference of Parasitic Light

The ability of parasitic light to interfere with the IC recovery from LDPs, as observed in the laser tests, was similarly demonstrated by the circuit simulations. We proceeded to examine three laser exposition conditions: no irradiation but with parasitic illumination, irradiation in the dark (without parasitic illumination), and irradiation under parasitic illumination. From the results shown in Fig. 7, we see that we are very consistent with the experimental data, with case 1 not perturbing the operations

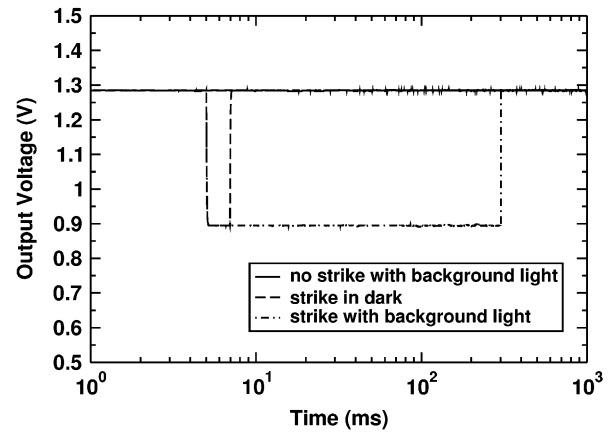


Fig. 7. Circuit simulation showing the modulating effects of parasitic light illumination on the width of LDPs. The strike with a background illumination is almost two orders of magnitude longer than the strike in the dark (3 ms versus 270 ms).

of the LM6144, but cases 2 and 3 doing so. Most importantly, we see that the background photocurrent (1 nA), applied to the sensitive area in addition to the simulated energetic strike, considerably extended the time to recovery (from a few milliseconds to 250 ms). The reason for this observation is that leakage currents, naturally present in these bipolar transistors, were favoring the circuit recovery by slowly eliminating the excess charge; perfect transistors would have helped maintain that charge indefinitely thus the stable corrupted state. Now, the leakage currents are partially balanced by the background-induced photocurrent and this results in delaying the circuit recovery.

To address our previous concern about the discrepancy between the width of laser-induced LDPs and broadbeam-induced ones, we must get more familiar with the laser setup used to obtain the results of Fig. 3. The IXL laser uses an ultrafast optomechanical shutter to limit the laser beam leakage to a narrow temporal window around the main laser impulse. However, even with an optimal installation and synchronization to the rest of the experimental apparatus, the sensitivity of the surface junctions is such that the shutter-limited leakage is still enough to induce important delay in the IC recovery (note that these junctions appeared to be sensitive even to ambient room light). This shows that surface junctions of delidded DUTs can be quite sensitive, advising that any further ion testing should be performed in the dark to avoid interference from stray light.

### C. Laser-Induced LDP Recovery

Our modeling results are able to explain the recovery of the LM6144 output voltage from the corrupted LDP state when the region surrounding the sensitive area was irradiated with the pulsed laser. By mapping the area on the photomicrograph (Fig. 2) to the elements of the circuit schematic (Fig. 4), we identified that the surroundings of the sensitive NPNs are implemented by the transistors Qp1, Q3, and Q4 (simplified as a current source), all turned off when the control biased are destabilized. The second laser strike jump-starts the slow excess charge leakage process by turning these transistors ON and re-establishing current flow through the critical resistors tied to the positive and negative outputs of the bias/startup circuitry.

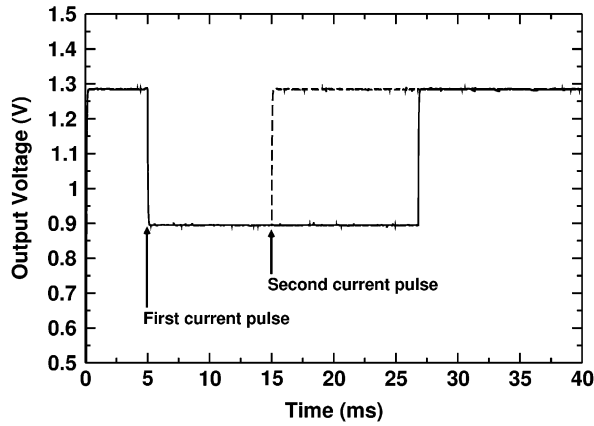


Fig. 8. Simulation of the effects of a laser strike in the vicinity of the sensitive area while the output voltage is experiencing an LDP. The figure illustrates a strike on Q3 but identical results were achieved with Qp1 and Q4.

The  $V_n$  and  $V_p$  control voltages recover almost immediately, shortly followed by a recovery of the LM6144 output (Fig. 8).

#### D. LDP Width Dependence on Power Supplies

The LDP width dependence on the amplitude of the power supplies, as observed during the laser tests, can also be explained. We have seen from the previous analyses that the recovery process is based on two dynamic processes: how fast can the excess charge deposited by the ion strike be leaked and how much current can be restored through the resistors tied to the output nodes  $V_n$  and  $V_p$ . Clearly, operating at higher supplies is favoring a faster recovery since the laser-induced photocurrents result in a relatively smaller perturbation of the quiescent currents. Also, higher currents will turn on OFF-transistors faster, allowing voltages to develop across the critical resistors more promptly.

### VI. SOLUTION FOR CIRCUIT RADIATION HARDENING

Using the results of our investigation on LDP triggering mechanisms, we present a circuit design modification with the purpose of achieving an acceptable level of LDP phenomenon mitigation.

Note that we are not trying to mitigate this effect exclusively in the LM6144 op amp, which is an already established part with a fairly low rate of LDP occurrence in a natural radiation environment: calculations with CREME 96 for Galactic Cosmic Rays during solar minimum (worst case) behind 100 mil of Al shielding on a GEO orbit, considering a critical charge of 20.5 pC, a sensitive area of  $3e-4 \text{ cm}^2$  and a thickness of  $10 \mu\text{m}$ , resulted in a rate of  $6.5E-7$  LDP/day. Instead, we are using this IC to develop a scheme to be applied in future analog designs with similar multistable circuitries, where power supply and scaling constraints may result in lower thresholds. These ICs will be more prone to exhibit the same type of anomalous LDP responses, but with a rate of occurrence that may be unacceptable for the survivability of the mission.

Instead of attempting to filter the event at the output of the IC and limit its propagation to any subsequent circuit or system (most commonly used method), we will act at the location of origination, i.e., the bias/startup circuit. The addition of a small

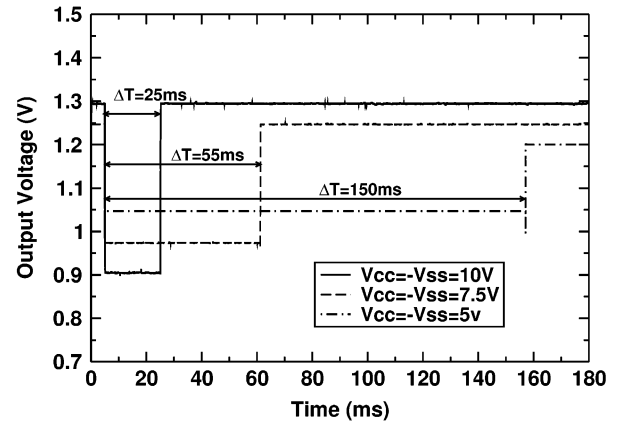


Fig. 9. Simulation of the influence of power supplies on the width of the LDPs. The saturating amplitude decreases with decreasing  $V_{cc}$  but the pulse width increases drastically.

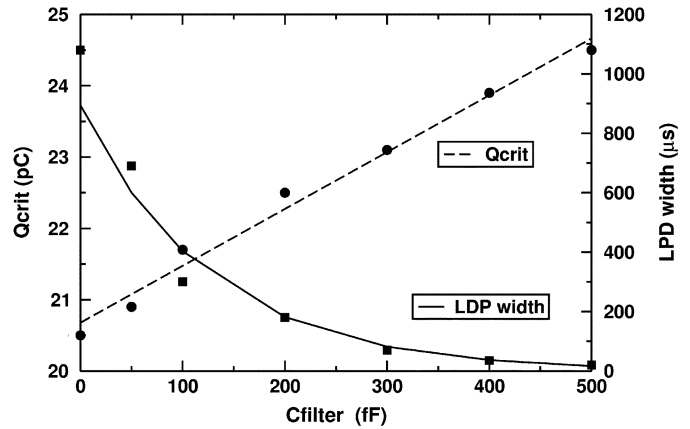


Fig. 10. Simulated evolution of the critical charge necessary to the onset of a LDP ( $Q_{crit}$ ) and the LDP pulse width as a function the capacitance value used for the radiation hardening solution ( $C_{filter}$ ).

capacitance between the collector and base terminals of each of the transistors Qp1 and Qp2 implements two low-pass filters enhanced through the Miller effect. The purpose of these capacitances is to filter the initial current glitches causing the base currents of these transistors to decrease, ultimately leading to bias destabilization because of the critical feedback loop with Qs1. Such modifications have a minimal effect of the performances of the LM6144 because they are implemented in a portion that has a static function: once the startup current is set and the circuit is biased, the bias/startup circuitry does not contribute to active operation of the IC. Fig. 9 shows the improvements in the LM6144 ASET response following this design modification.

The additions of the CE capacitances ( $C_{filter}$ ) have two beneficial consequences.

- 1) The critical charge necessary to the onset of a LDP can be increased. For a  $C_{filter}$  value of 500 fF, the  $Q_{crit}$  increases 20% (from 20.5 to 24.5 pC). So the circuit will require ions with an even higher LET to enter a corrupted stable mode.
- 2) The width of a LDP can be reduced to acceptable durations, making it compatible with any system-level ASET mitigation technique that would be already implemented in the on-board system. Fig. 10 shows that, for an injected

charge of 24.5 pC, the width on the resulting LDP can be modulated from 1.1 ms to 20  $\mu$ s. The choice of the latest pulse width is not random: 20  $\mu$ s has been estimated as the worst-case pulse width for SETs in analog ICs [8]. From this work, it is clear that ASET events with characteristics far outside established worst-case estimations can occur.

## VII. SUMMARY AND CONCLUSION

This work presents the investigation of a new category of ASETs characterized by millisecond-long pulse widths. First observed during heavy-ion tests on the LM6144, these long duration pulses were confirmed by pulsed lasers and their location of origination identified on the IC. ASET computer simulation was used to model the phenomenon, and combined with experimental observations, revealed that a radiation-induced stable circuit state was responsible for the latch-like response of the LM6144.

This finding can have potential implications to other circuits with similar multimode bias topologies, where exposition to ionizing radiation can inadvertently switch the IC into unreliable operation. Therefore, we presented a design solution, based on the implementation of a low-pass filter in the critical feedback loops of the bias/startup circuit to mitigate the LDP occurrences in this IC, but such concept can be extended to harden future analog designs with similar topologies. We have also seen that surface junctions can be very photosensitive, so the irradiation of delidded parts should be performed in the dark, to avoid interfering photocollection effects. With these new results, we may need to reevaluate what was considered as worst-case ASET in analog ICs (20  $\mu$ s pulse width) from which hardness assurance methodologies were developed.

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